What is claimed is:

1. A semiconductor memory device comprising:

a plurality of memory cell arrays, each of which include a plurality of memory cells in a matrix;

a mode control unit which outputs a delay control signal;

an instruction execution unit which accesses to said plurality of memory cells based on an address and an address buffer control signal supplied externally; and

a command control unit which outputs said address buffer control signal to said instruction execution unit based on a command supplied externally and said delay control signal,

wherein said command control unit outputs said address buffer signal in synchronization with a clock signal when said delay control signal is in an inactive state and said command is a write command or a read command in an ordinary operation mode, and

when said delay control signal is in an active state and said command is said write command in a write instruction delay operation mode,

wherein said command control unit outputs said address buffer signal delayed compared with said clock signal when said delay control signal is in the active state and said command is said read command in a read instruction delay operation mode.

2. The semiconductor memory device according to claim 1, wherein said command control unit outputs a command signal of the active state in synchronization with said clock signal to said instruction execution unit when said command is said write command and outputs a command signal of the inactive state in synchronization with said clock signal to said instruction execution unit when said command is said read command, and

wherein said instruction execution unit accesses to said memory cell array based on said address, said address buffer control signal and said command signal.

3. The semiconductor memory device according to claim 2, wherein said command control unit comprises a command decoder circuit which comprises:

a control unit which inputs said command supplied externally, and outputs said command signal in synchronization with a first clock signal and outputs said address buffer control signal in synchronization with a second clock signal;

a delay circuit which outputs said address buffer control signal delayed;

a multiplexer circuit which selects and outputs one of said address buffer control signal and said

address buffer signal delayed by said delay circuit based on said delay control circuit and said command signal to said order execution unit.

4. The semiconductor memory device according to claim 2, wherein said instruction execution unit write a data based on said address buffer control signal when said command signal is in the active state.

5. The semiconductor memory device according to claim 2, wherein said instruction execution unit reads a data from said address based on said address buffer control signal when said command signal is in the inactive state.

6. A method of a memory access to a plurality of memory cell arrays each of which includes a plurality of memory cells comprising:

generating a delay control signal;

generating an address buffer control signal in synchronization with a clock signal when said delay control signal is in an active state and a command is a write command in a write instruction delay operation mode;

delaying said address buffer control signal

from said clock signal when said delay control signal is in the active state and said command is a read command in a read instruction delay operation mode; and

accessing to said plurality of memory cell arrays based on an address supplied externally and said address buffer control signal.

7. The method according to claim 6, further comprising:

generating said address buffer control signal in synchronization with said clock signal when said delay control signal is in an inactive state and said command is said write command or said read command in an ordinary operation mode.

8. The method according to claim 7, further comprising:

generating said command signal of an active state in synchronization with said clock signal when said command is said write command;

generating said command signal of an inactive state in synchronization with said clock signal when said command is said read command, wherein said accessing includes accessing to said plurality of memory cell arrays based on said address buffer control signal and said command signal.

9. The method according to claim 8, wherein said accessing includes writing a data in said address based

on said address buffer control signal when said command signal is in the active state.

10. The method according to claim 8, wherein said accessing includes reading the data from said address based on said address buffer control signal when said command signal is in the inactive state.